IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.(Currently Amended) A data processing apparatus, the apparatus comprising:

an instruction addressing unit;

an instruction memory system arranged to output an instruction word, capable of containing a plurality of instructions, in response to an instruction address from the instruction addressing unit, the instruction memory system comprising a plurality of memory units, arranged to output respective parts of the instruction word in parallel;

an instruction execution unit, comprising a plurality of functional units, each capable of executing a respective instruction from the instruction word in parallel with execution of other instructions from the instruction word by other ones of the

functional units;

an instruction address modification circuit arranged to modify translation of the instruction address into a physical address for a particular one of the memory units relative to other ones of the memory units and to change generation of instruction words from instructions from different memory units during execution of a program, the instruction address modification circuit being configured to modify an address translation between supplying a first instruction address for a first instruction word and supplying a second instruction address for a second instruction word, the second instruction word being different from the first instruction word and including a copy of a part of the first instruction word, so that the part of the first instruction word is re-used in the second instruction word thereby reducing memory needed to store the program,

wherein the instruction address modification circuit includes an offset register which is directly connected to an output of a functional unit of the plurality of functional units, the functional unit updating an offset value in the offset register

during the execution of the program, and

wherein the instruction address modification circuit is operationally coupled to a controller that provides the instruction address, and to one of the plurality of the functional units that provides an adjust signal to the instruction address modification circuit, and wherein the controller is distinct from the functional unit; the instruction address modification circuit being configured to modify the translation in response to the adjust signal and to provide a modified translated address to one of the plurality of the memory units.

2.(Previously Presented) The data processing apparatus according to Claim 1, wherein the instruction address modification circuit is arranged to modify the translation under control of a modification update instruction from the instruction word during program execution.

3.(Previously Presented) The data processing apparatus according to Claim 2, wherein the particular one of the memory

units is arranged to supply instructions exclusively to a group that contains a subset of the functional units, the group containing a modification update functional unit constructed to execute the modification update instruction.

4.(Previously Presented) The data processing apparatus according to Claim 2, wherein the particular one of the memory units is arranged to supply instructions exclusively to a group that contains a subset of the functional units, the functional units comprising a modification update functional unit outside the group constructed to execute the modification update instruction.

5.(Previously Presented) The data processing apparatus according to Claim 2 wherein the modification update instruction is a conditional instruction, the modification update being executed dependent on fulfillment of a condition specified in the modification update instruction.

6.(Previously Presented) The data processing apparatus

according to Claim 1, wherein the instruction address modification circuit is arranged for instruction address and memory unit dependent address translation, so that a first and a second instruction address are translated to a same physical address for the particular one of the memory units and to mutually different physical addresses for one or more memory units other than the particular one of the memory units.

7.(Previously Presented) The data processing apparatus according to Claim 1, programmed to use repeated modification of said translation to repeatedly output one or more instructions making up a loop of instructions, while the instruction address progresses so that the instructions from the loop are combined in the instruction words with progressive instructions that are not repeated during at least part of the repetitions of supply of instructions from the loop.

8.(Previously Presented) The data processing apparatus according to Claim 2, programmed to use said modification update

instruction to selectively output, dependent on a data dependent condition, a first or a second block of one or more instructions from said particular one of the memory units, while the instruction address progresses so that at least part of the memory units output one or more instructions from a third block of instructions as part of the instruction word or words in combination with instructions from said first or second block.

9. (Previously Presented) The data processing apparatus according to Claim 1, wherein a first number of addressable instruction addresses of the particular one of the memory units differs from a second number of addressable instruction addresses of at least one of the memory units.

10. (Previously Presented) The data processing apparatus according to Claim 9, wherein the particular one of the memory units is arranged to switch to a power saving state when the modified instruction address is outside an address range or set of address ranges that contains said first number of instruction

addresses.

11. (Currently Amended) A method of executing a program of instruction words with a data processing apparatus that comprises a plurality of functional units capable of executing a plurality of instructions from each instruction word in parallel, wherein the instructions from each of at least some of the instruction words are fetched from respective memory units in parallel, the method comprising the acts of:

addressing the instruction word with an instruction address that is common for the functional units;

using a modifiable translation of the instruction address into a physical address for a particular one of the memory units to select dependent on program execution which instructions from the memory units will be combined into the instruction word in response to the instruction address;

modifying an address translation between supplying a first instruction address for a first instruction word and supplying a second instruction address for a second instruction word, the

second instruction word being different from the first instruction word and including a copy of a part of the first instruction word, so that a part of the first instruction word is re-used in the second instruction word thereby reducing memory needed to store the program; and

connecting an output of an offset register to an offset adder, the offset adder being connected between a controller that provides the instruction address and the particular one of the memory units;

wherein the modifying act includes updating, by a functional unit of the plurality of functional units, an offset value in the offset register during the execution of the program, the offset register being directly connected to an output of the functional unit, and the controller being distinct from the functional unit.

12. (Previously Presented) The method of executing a program of instruction words according to Claim 11, wherein the modifiable translation is selected under control of a modification update instruction in the program.

13.(Previously Presented) The method of executing a program of instruction words according to Claim 11, comprising modifiable translation to repeatedly fetch instructions from a loop from repeated physical addresses in a particular one of the memory units in response to progressive instruction addresses, so that the instructions from at least part of repetitions of the loop are combined in the instruction words with progressively different instructions memory units other the than the particular one of the memory unit.

14.(Original) A computer program product comprising instruction words, each for execution in one or more respective instruction cycles by a data processing apparatus according to Claim 2, the instruction words comprising at least one modification update instruction for causing the data processing apparatus to execute, upon addressing a first one of the instruction words, a combination of instructions from the first one of the instruction word with further instructions from outside the first instruction word, following execution of the modification update word.

Claims 15-16 (Canceled)

17.(Previously Presented) The method of claim 11, wherein the modifying act is performed in response to an adjust output from one of the plurality of the functional units.

18.(Previously Presented) The data processing apparatus of claim 1, wherein an output of the offset register is connected to an offset adder, the offset adder being connected between the controller that provides the instruction address and the particular one of the memory units.

19.(Previously Presented) The data processing apparatus of claim 1, wherein the functional unit updates the offset value during the execution of the program dependent on conditions that occur during execution.

Claim 20 (Canceled)